CLAIMS

1. A wireless transceiver device, comprising:

modulation circuitry for modulating and demodulating signals that are transmitted over the airwaves;

frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals;

digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog;

a radio controller; and

baseband processing circuitry including a first in, first out memory structure for storing addresses for accessing data blocks.

2. The wireless transceiver of claim 1 further including a plurality of command blocks formed within a memory structure, which command blocks include addresses of data blocks stored within random access memory.

3. The wireless transceiver of claim 2 wherein the first in, first out memory structure includes pointers that define addresses of the command blocks.

4. The wireless transceiver of claim 2 further forming a memory portion for storing an indicator for indicating whether a command block is in use.

5. The wireless transceiver of claim 1 wherein the modulation circuitry includes GPSK modulation and demodulation circuitry.

6. The wireless transceiver of claim 1 wherein the frequency conversion circuitry converts directly between RF and baseband.

7. A method for storing and transmitting data, comprising:

storing a data block in random access memory; and

storing a pointer that corresponds to the data block in a first in, first out memory structure.

8. The method of claim 7 wherein the pointer comprises an address of a command block.

9. The method of claim 8 further including the step of storing an address of the data block in the command block.

10. The method of claim 9 further including the step of setting a signal in a defined memory location, which signal indicates that the address in the command block is for data that has yet to be successfully transmitted and therefore that the command block is busy.

11. The method of claim 10 wherein an address for a data block is only stored in a command block if an indicator reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted.

12. The method of claim 7 further including the step of evaluating a command block address stored within a FIFO pointer.

13. The method of claim 12 further including examining the contents of the command block specified by the pointer to determine a data block address.

14. The method of claim 13 further including the step of evaluating at least the first memory location of the data block whose address is specified in the command block to determine the size of the data block.

15. The method of claim 14 further including the step of retrieving an amount of data corresponding to the size data block specified in claim 14 and transmitting that data to a radio modem for transmission over a wireless airwaves.

16. The method of claim 15 further including the step of resetting the indicator signal if the transmission was successful.

17. A memory structure formed within a baseband processing system, comprising:

a random access memory portion for storing data blocks that are to be transmitted in a first in, first out order; and

a first in, first out memory structure for storing pointers that correspond to the data blocks.

18. The memory structure of claim 17 wherein a plurality of command blocks are defined within the random access memory wherein each command block is for specifying an address of a data block that is to be transmitted.

19. The memory structure of claim 18 further including a defined memory portion for storing command block indicators for each command block, which indicators specify whether its corresponding command block includes the address of a data block that has yet to be transmitted successfully.

20. The memory structure of claim 19 wherein the memory portions for storing the indicators are each one bit in length.

21. The memory structure of claim 18 wherein the memory portions for storing the command blocks are each four bytes in length.

22. The memory structure of claim 17 wherein the first in, first out memory structure defines a plurality of first in, first out memory blocks wherein each first in, first out memory relates to data blocks that are to be transmitted to a particular device.